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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,187	12/20/2001	Murari Kejariwal	1248-CIC (P176US)	9680

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EXAMINER	
NGUYEN, TUNG X	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/027,187	KEJARIWAL ET AL.	
	Examiner	Art Unit	
	Tung X Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *the amendment filed on 8/27/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 6* is/are rejected.

7)☐ Claim(s) *2 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of group I with species of figures 1-6 including claims 1-6 filed on 8/27/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-4, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Browen et al. (u.s.p 6,327,545), in view of Shibuya et al. (u.s.p Re. 34,295).

Regarding to claim 1; Brown et al teaches method and apparatus for testing an integrated circuit comprising the step of:

- A circuit under test (110 of figure 1) having a plurality of integrated circuit, transistor, ... (col. 1, lines 40-45), wherein the integrated circuit (figure 1) having a plurality of nodes (figure 1). Therefore, Browen et al. disclose the step of observing a selected parameter at a selected test node in the circuit under test (110 of figure 1).
- Detector considered to be a measurement hardware (106 of figure 1) for detecting tested node signal on the plurality of nodes of circuit under circuit (figure 1),

and generating the tested node signal to a fault analysis (108) for detecting and analyzing pass or fail of the test nodes; and

- The fault analysis (108), is coupled to a circuit model (102) of a test program generator (104), for comparing and analyzing the reference voltage with the tested signal from the node of circuit under test. See figures 1-16.

Brown et al teaches all of features of claimed invention except for reference current. However, Shibuya et al teaches that it was known in the art to provide a device for detecting CMOS IC circuit (14) comprises a reference current (20a figure 1) of a comparator (24 of figure 1) to compare tested signal of CMOS IC circuit (14 of figure 1). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Browen et al., and provide the comparator since it is well known in the art as taught Shibuya et al., for the benefit of detecting the integrated circuit pass/fail status (col. 2, lines 50-60).

Regarding to claim 3, Browen et al. disclose the Fautl analysis (108 of figure 1) for allowing test nodes of the circuit under test for comparing an initial level considered to be a minimum value (col. 16 lines 15-25) of the reference voltage/current of the circuit model (102, 104 figure 1).

As to claim 4, Shibuya et al. disclose the differential voltage (24 of figure 1).

As to claim 6, Shibuya et al. disclose the step of initiating a test mode in response to power-up of the integrated circuit (fig. 7)

Allowable Subject Matter

4. Claims 2, 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claims 2, 5, the prior art does not teach the stepping the current to the integrated circuit by a second selected step representing the second error, the current being a sum of the selected step and the second selected current step and representing the error and the second error; in combination with the other claimed features.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6320275 B1, US 5999008 A, US 5559454 A are related to the method and apparatus for testing the integrated circuit, using the detector for detecting passed/failed integrated circuit.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN
9/07/04

Ashok Kumar Sridhar
9/17/04